Electronic Version
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Claims

[c1] 1. A multi-chip package structure, comprising:
a carrier with a surface;
at least a package module positioned on the surface of the carrier, wherein the package module has a plurality of chips, at least two of which are stacked;
an insulation layer positioned on the surface of the carrier enclosing the package module, wherein the insulation layer has a plurality of first via holes linked to the surface of the carrier, and a depth of the first via hole in a direction perpendicular to the surface of the carrier is greater than a height of the package module in the same direction; and
a patterned metallic layer positioned on the insulation layer and filling the first via holes, wherein the patterned metallic layer serves as interconnecting lines inside the multi-chip package.

[c2] 2. The multi-chip package of claim 1, wherein the package further comprises a plurality of contacts attached to the surface of the carrier and enclosed within the first via holes so that the patterned metallic layer and the carrier are electrically connected through the contacts.

[c3] 3. The multi-chip package of claim 1, wherein the stacked chips within the package module are joined together using a flip chip bonding technique.

[c4] 4. The multi-chip package of claim 1, wherein the insulation layer has a plurality of second via holes linked to at least one of the chips of the package module, and the patterned metallic layer fills the second via holes.

[c5] 5. The multi-chip package of claim 4, wherein the package further comprises a plurality of contacts attached to at least one of the chips and enclosed within the second via holes such that the patterned metallic layer and at least one of the chips are electrically connected through the contacts.

[c6] 6. The multi-chip package of claim 1, wherein the carrier is a chip.

[c7] 7. The multi-chip package of claim 1, wherein the carrier is an integrated circuit package substrate.

[c8] 8. A process of fabricating a multi-chip package, comprising the steps of:
providing at least a package module and a carrier, wherein the package module has a plurality of stacked chips;

attaching the package module to a surface of the carrier;
forming a first insulation layer on the surface of the carrier so that the package module is enclosed;
forming a plurality of first via holes that passes through the first insulation layer and links to the carrier;
forming a patterned metallic layer over the first insulation layer and filling the first via holes, wherein the patterned metallic layer serves as interconnecting lines inside the multi-chip package; and
forming a second insulation layer over the metallic layer, wherein the second insulation layer has a plurality of openings that exposes a portion of the metallic layer.

[c9] 9. The process of claim 8, wherein the process further comprises attaching a plurality of contacts on the surface of the carrier within the first via holes.

[c10] 10. The process of claim 8, wherein the stacked chips within the package module are connected using a flip chip bonding technique.

[c11] 11. The process of claim 8, wherein the process further comprises forming a plurality of second via holes in the first insulation layer and linked to at least one of the chips of the package module and the patterned metallic layer fills the second via holes.

[c12] 12. The process of claim 11, wherein at least one of the chips of the package module has a plurality of contacts located within the second via holes, and the patterned metallic layer and the chip are electrically connected through the contacts.

[c13] 13. The process of claim 8, wherein the carrier is a chip.

[c14] 14. The process of claim 8, wherein the carrier is an integrated circuit package substrate.

[c15] 15. The process of claim 8, wherein before attaching the package module to the surface of the carrier, the process further comprises electrically testing the package module.

[c16] 16. A multi-chip package structure, comprising:
a carrier with a surface;
at least a package module positioned on the surface of the carrier, wherein the package module has a plurality of chips, at least two of which are stacked;
a first insulation layer positioned on the surface of the carrier enclosing the package module, wherein the first insulation layer has a plurality of first via holes linked to the surface of the carrier and a second via holes linked to at least one of the chips in the package module, and a depth of the first via hole in a direction perpendicular to

the surface of the carrier is greater than a height of the package module in the same direction;

a patterned metallic layer positioned on the first insulation layer and filling the first via holes and the second via holes, wherein the patterned metallic layer serves as interconnecting lines inside the multi-chip package;

a second insulation layer positioned over the metallic layer, wherein the second insulation layer has a plurality of openings that exposes a portion of the metallic layer; and

a plurality of first contacts deposited on the metallic layer exposed by the openings of the second insulation layer.

[c17] 17. The multi-chip package of claim 16, wherein the package further comprises a plurality of second contacts attached to the surface of the carrier and enclosed within the first via holes, and the patterned metallic layer and the carrier are electrically connected through the second contacts.

[c18] 18. The multi-chip package of claim 16, wherein the stacked chips within the package module are joined together using a flip chip bonding technique.

[c19] 19. The multi-chip package of claim 16, wherein the package further comprises a plurality of third contacts

attached to at least one of the chips and enclosed within the second via holes, and the patterned metallic layer and at least one of the chips are electrically connected through the third contacts.

[c20] 20. The multi-chip package of claim 16, wherein the carrier is a chip.

[c21] 21. The multi-chip package of claim 16, wherein the carrier is an integrated circuit package substrate.